REMARKS

Claims 1-13 and 18-21 are pending in this application, of which Claims 1, 7, 12, and 18 are the independent claims. All claims stand rejected.

Claim 18 is being amended to further clarify the scope of the claimed subject matter, by reciting "means for conveying the portions of the packets to the memory array portion in parallel, concurrent with receiving other packet data to the serial registers." Support for this amendment is found at least on page 13, lines 10-22 of the specification as originally filed. Acceptance is respectfully requested.

Rejection of Claims 1-13 and 18-21 under 35 U.S.C. 102(b) and 35 U.S.C. 103(a)

Claims 1-13 and 18-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Joffe (U.S. Patent No. 5,440,523) in view of one or more of Toda and Zuravleff. Applicants respectfully disagree with these rejections and request reconsideration.

Claim 1 is directed to a packet buffer random access memory (PBRAM) device. An example PBRAM device is illustrated in Fig. 7, where the PBRAM device 62 includes a memory array 74, a plurality of input ports 70 (I/O Port 0 – I/O Port 31), and a plurality of serial registers 72 associated with the input ports 70 (serial register 0 – serial register 31). The serial registers 72 each receive packet data from one of the associated ports 70 and write the packet data to the memory array 74 (see Specification, page 4, lines 3-11). Each of the serial registers 72 is further segmented into a plurality of segments, each segment being associated with corresponding portions of the memory array 74. Such a configuration is illustrated in Fig. 8, where a serial register 72 is divided into segments of 256 bits each. Further, a segment of the serial register 72 may transfer data into the memory 74 concurrent with another segment of the serial register 72 receiving other data (page 13, lines 11-15).

In the Office Action, section "Response to Arguments," it is stated that "Applicants arguments with respect to Claims 1 and 12 have been fully considered but are moot in view of the new ground(s) of rejection." Applicants understand the new grounds of rejection, as distinguished from the rejections presented in the previous Office Action, to be as follows:

> Toda et al discloses a...serial register configured for receiving packet data from the associated input port concurrent with writing other packet data to the memory

> array (see Figure 16 and see column 12 lines 21-24; lines 30-34 and Figure 17; Din which donates the access operation from data input to the memory through the serial register). [Office Action, page 3, lines 7-14; emphasis added.]

Contrary to the above assertion, however, Toda does not disclose any such feature. With regard to the particular text and Figures cited above:

Col. 12, lines 21-24, with reference to Fig. 16, describes a data transfer operation between the memory cell groups 162 and the data I/O section 164. It states that such an operation "is performed through the eight serial registers [167] at a time." This statement means that a data transfer, such as reading from (or writing to) the memory cell 162, is completed by moving the data through the eight serial registers 167.

Col. 12, lines 30-34, further describes the data transfer. For transfer between the memory cell groups 162 and the serial register section 167, "eight bit data is transferred at once." For transfer between the data I/O section 164 and the serial register section 167, "the eight bit data is seriously [*sic*] transferred." In other words, data is transferred in parallel to/from the memory cell 162, and is transferred serially to/from the data I/O section 164. Toda makes clear that the parallel transfer and the serial transfer are merely two different types of data transfer (col. 12, lines 27-28). Toda does <u>not</u> state that both transfers can occur concurrently. On the contrary, it is impossible for a parallel and a serial transfer to occur concurrently, because in a parallel data transfer, every portion of the serial register section 167 is used to transfer data (col. 13, lines 1-6). A data transfer control section 168, as shown in Fig. 16, selects between parallel and serial transfer operations, which ensures that both do not occur concurrently (col. 12, lines 27-28). Thus, during a parallel transfer, the serial register section 167 is not available for serial transfer.

In Fig. 17, Toda discloses a timing diagram for data input and data output operations. Signal Dout represents signals <u>from</u> the data I/O section 164 during a data <u>output</u> operation (col. 12, lines 63-65). Signal Din represents signals <u>to</u> the data I/O section 164 during a data <u>input</u> operation (col. 12, lines 66-67). As Toda makes clear, the data input and data output operations do not occur concurrently. Rather, the data input and the data output are <u>two different cases</u>, and are both depicted in Fig. 17 to show the difference between them (col. 12, line 63 – col. 13, line 6). Moreover, if both cases occurred simultaneously, it would require the serial register section 167 to move data to and from the data I/O section 164 at the same time, which is not possible given Toda's serial configuration.

Thus, Toda does not disclose or suggest "receiving packet data from the associated input port concurrent with writing other packet data to the memory array," as recited in Claim 1 and in similar language in Claim 12. Claim 7 recites a similar feature, and thus the foregoing applies. Claim 18 as now amended also recites a similar feature. Claims 2-6, 7-11, 13 and 19-21 depend from one of Claims 1, 7, 12 and 18. As a result, the § 103 rejection of Claims 1-13 and 18-21 is believed to be traversed, and reconsideration is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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